Fast Sampling Front-End Via DRS 4 Switched Capacitor Array Information Note*

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Quick Features

64 channels on one 6 U VME board

700 MSPS to 5 GSPS sampling rate

2048 sampling cells per channel

1 mV low RMS noise after calibration

1 V single-ended input range

0.5×10^{-3} low integral nonlinearity

-40 dB crosstalk in adjacent channels

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Description

The DRS 4 chips is a fast-sampling front-end based on a Domino switch array, designed by Paul Scherrer Institute. This array generates a very fast Domino wave which could have its frequency controlled via the internal PLL and sample the analog input in the associated sampling capacitors. The sampling rate could be guaranteed between 700 MSPS and 5 GSPS or better for some selected chips. Each chip has (8+1) channels and each channel has 1024 sampling cells, which could be daisy-chained for larger sampling depth.

This 6 U VME board being presented is centered around 16 DRS 4 chips assembled on board. Each chip is running in the channel-daisy-paired mode so there are 64 sampling channels in total with 2048 sampling depth. In addition the 9th channel of every chip samples a high frequency LVDS clock which could be used to exact timing calibration of one sample.

The board receives single-ended input which is turned into differential via on-board transformers. This passive buffer limits the input bandwidth below the actual capacity of the DRS 4 chip, and further upgrades to active input buffers could improve it a lot. The input would be sampled in the chip cells and get read out at a trigger with all channels in parallel. The dead time is thus determined by the number of samples per readout and the readout clock frequency. A readout clock of 25 MHz is verified to be fine and an upgrade to 33 MHz clock may not pose a big problem.

Flexibility of the DRS4 chip allows maximum level of control over a sampling run. The sampling rate is locked by a programmable external reference clock and the actual sample number to read out every time is free for all, only limited by the sampling depth. The daisy-chaining of channels could also be adjusted on-line to achieve a larger sampling depth or channel density. The 16 DRS 4 chips are grouped into four blocks, 4 on each block. Therefore different blocks could run in different modes without any conflict. There is one programmable FPGA per block and in addition a global control FPGA providing all programmable control.

Specifications

Parameter	Typical	Unit	Comment
Analog Input			
Single-ended input span	1	V p-p	
Absolute input range	-0.55 - 2.05	V	
Input bandwidth (-3 dB)	200	MHz	Upgradable to 800 MHz with active input buffer
Adjacent channel crosstalk	$\leq$-40	dB	
Domino Sampling			
Sampling channels	64	channels	
Sampling depth	2048	samples	
Sampling rate	0.7	GSPS min	
	5	GSPS max	Guaranteed
	6	GSPS max	Selected DRS 4 chips
Samples per readout	0 - 2048	samples	Region of interest readout mode
Readout speed	25	MHz currently	Upgradable to 33 MHz
	40	MHz max	At reduced linearity
Fixed cell offset variation	8	mV rms	
Random noise	1	mV rms	After offset correction
Integral nonlinearity	0.5	mV	After offset correction
Effective number of bits	9.5		After offset correction
Dead time percentage	TBD	%	At 10 kHz trigger rate per channel
Power Consumption			
Power per channel	0.66	W/channel	DRS chips not running
	0.75	W/channel	DRS chips in standby at 1 GSPS
	0.79	W/channel	DRS chips taking data at 1GSPS

Illustrations

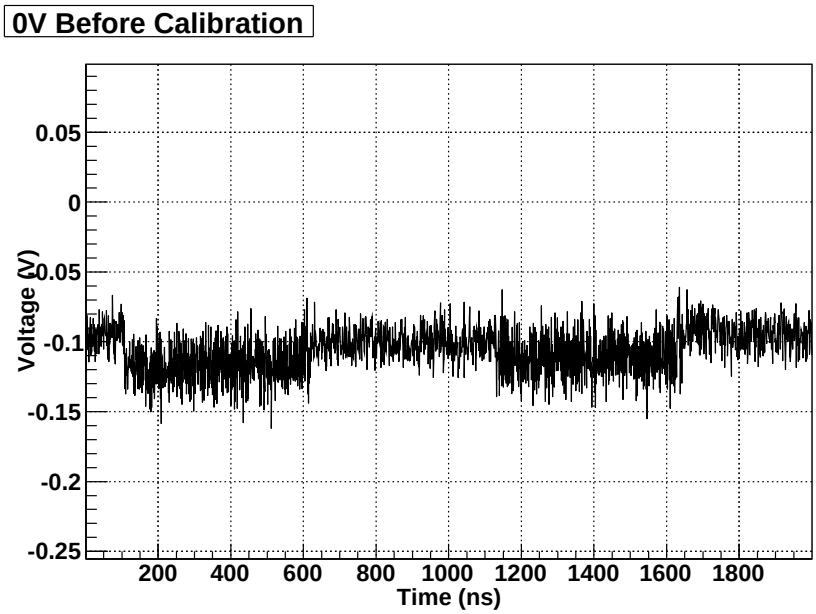

FIG. 1: 0V DC Signal Sampled At 1 GSPS Before Offset and Gain Calibration

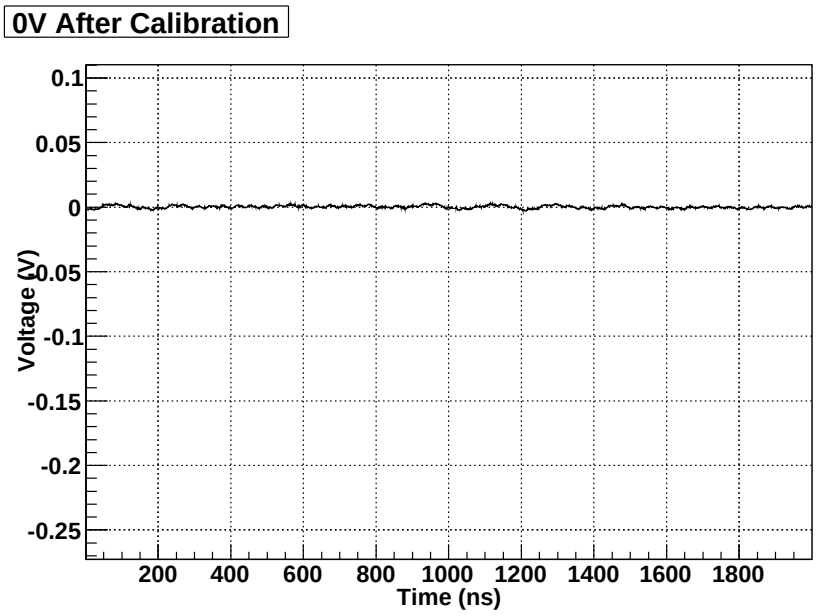

FIG. 2: 0V DC Signal Sampled At 1 GSPS After Offset and Gain Calibration

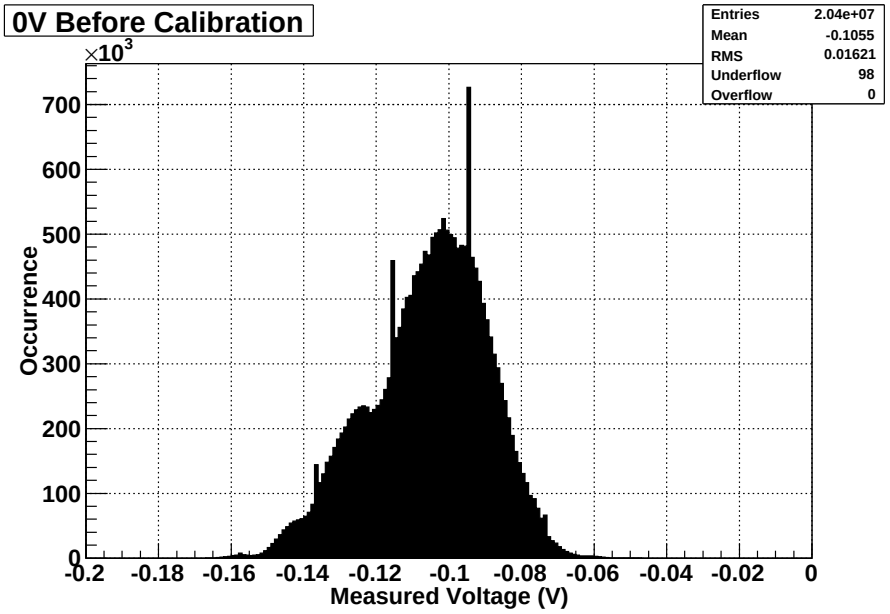

FIG. 3: Noise Histogram Before Offset and Gain Calibration

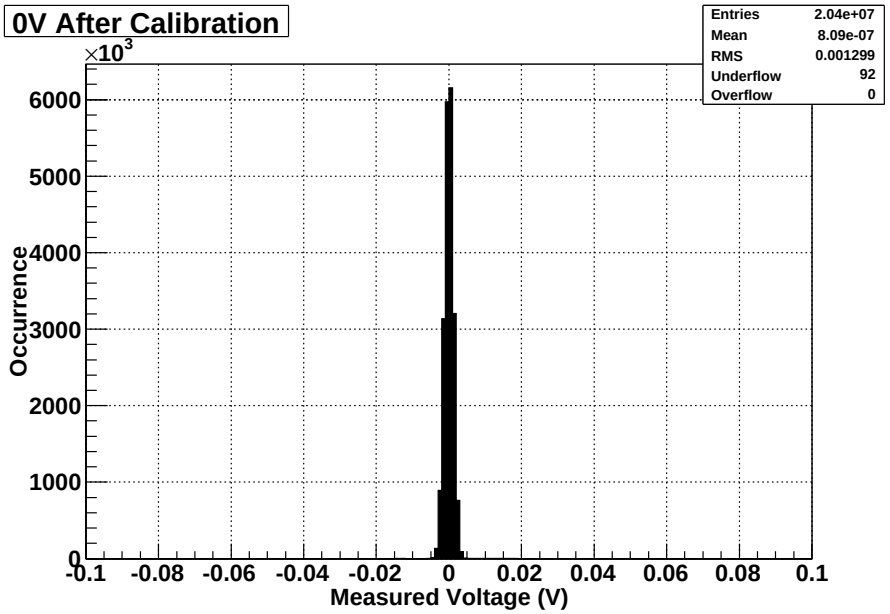

FIG. 4: Noise Histogram After Offset and Gain Calibration

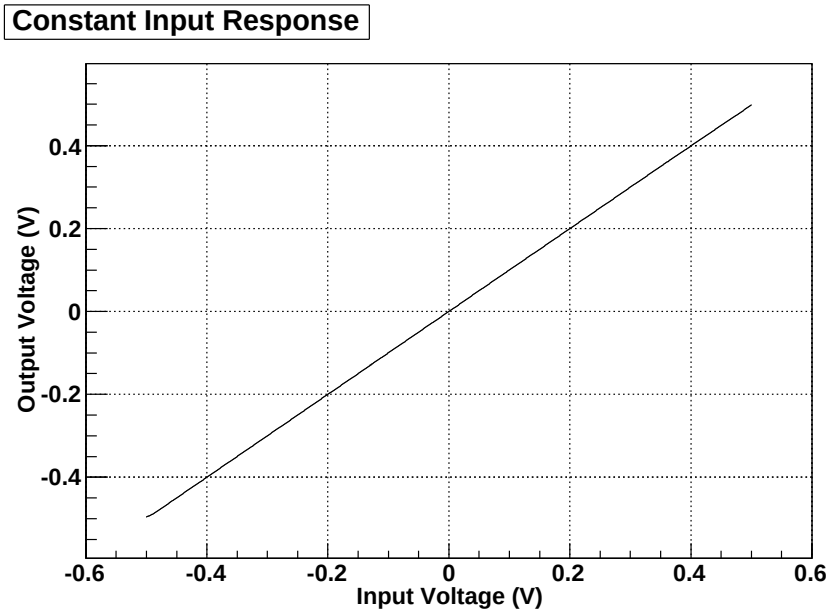

FIG. 5: Output vs. Input After Offset and Gain Calibration

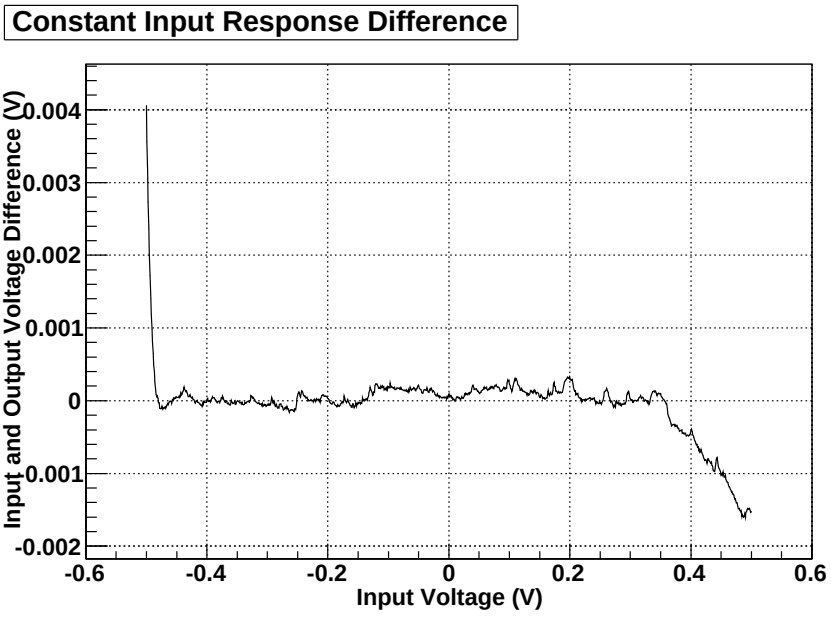

FIG. 6: Typical Nonlinearity After Offset and Gain Calibration

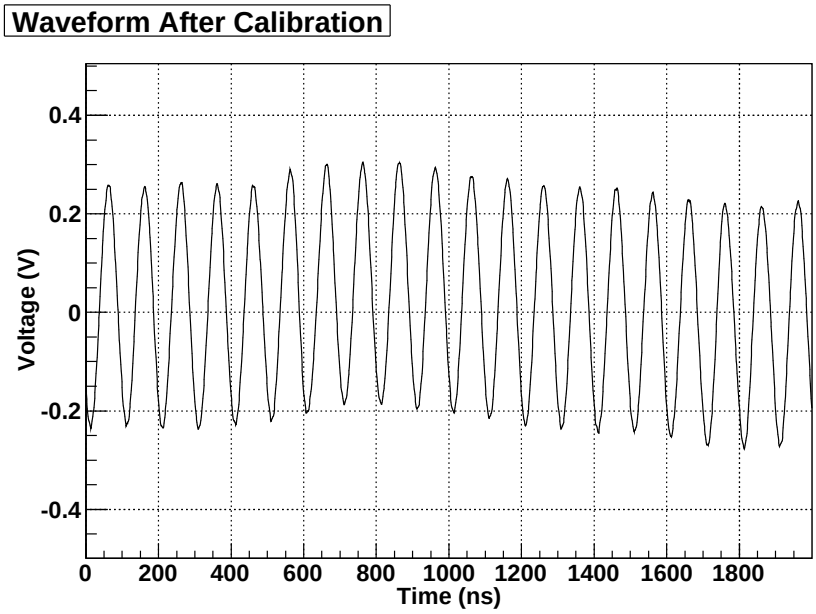

FIG. 7: 500 mV p-p, 10 MHz Sine Wave Sampled At 1 GSPS After Offset and Gain Calibration[a]

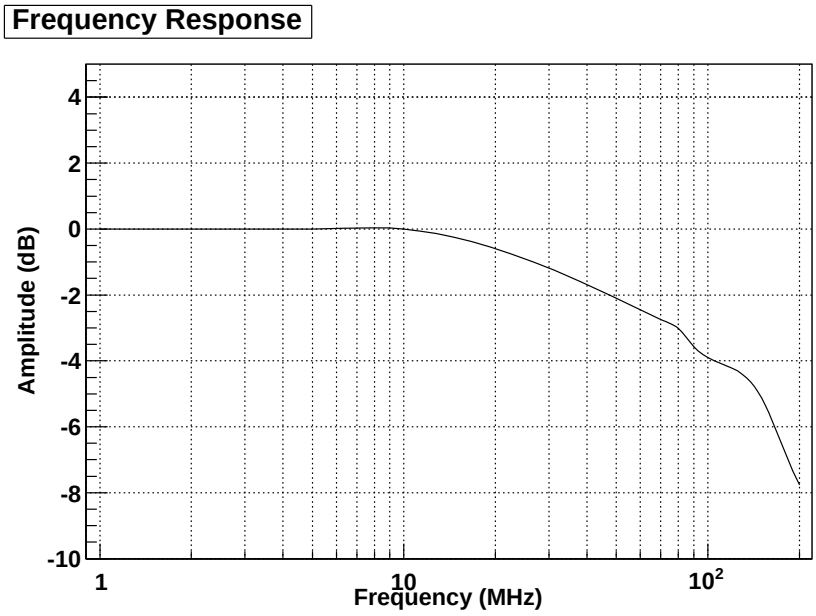

FIG. 8: Signal Frequency Response

[a] Fluctuations in the waveform are caused by deficiencies of the wave generator used.