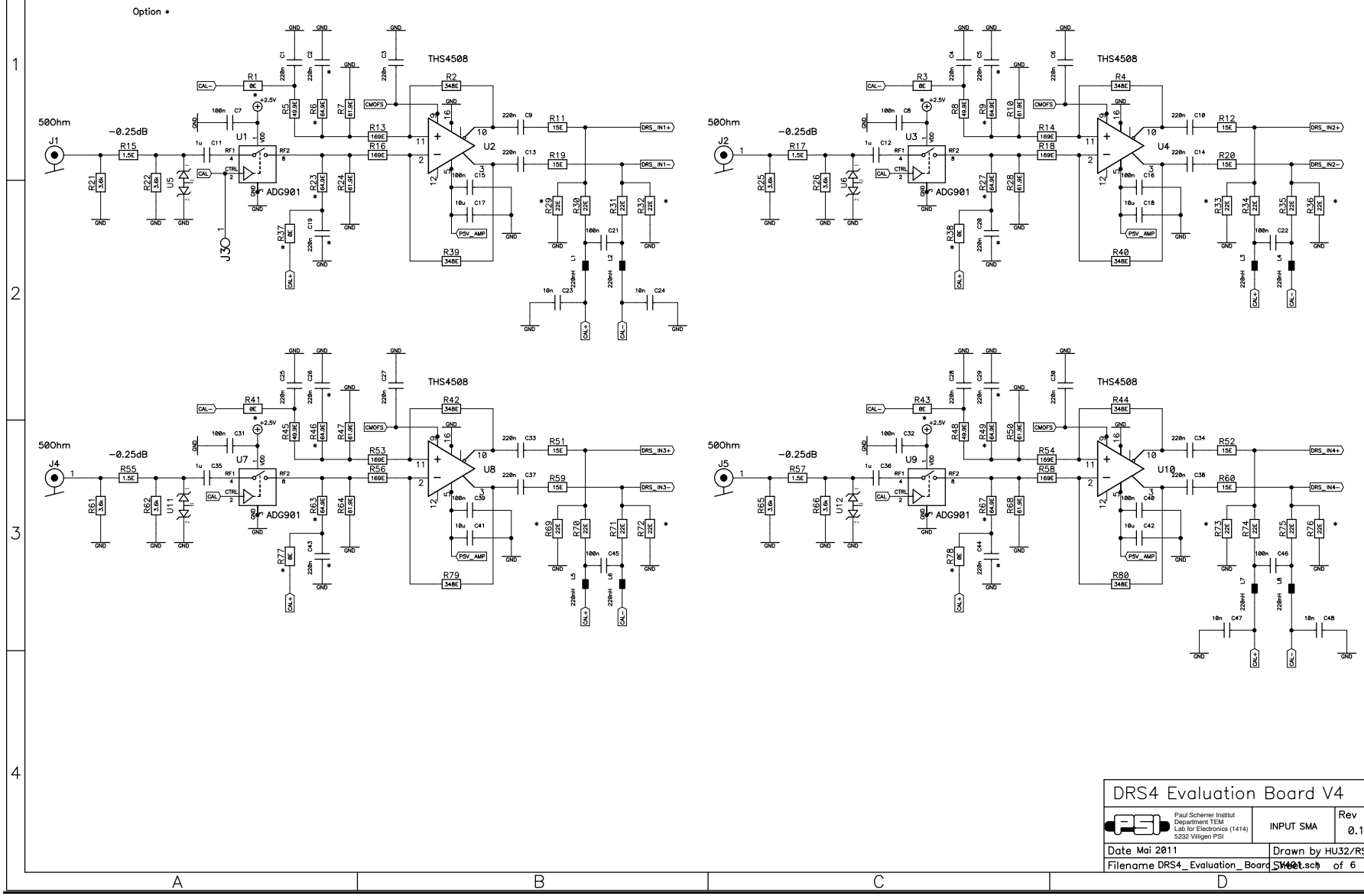
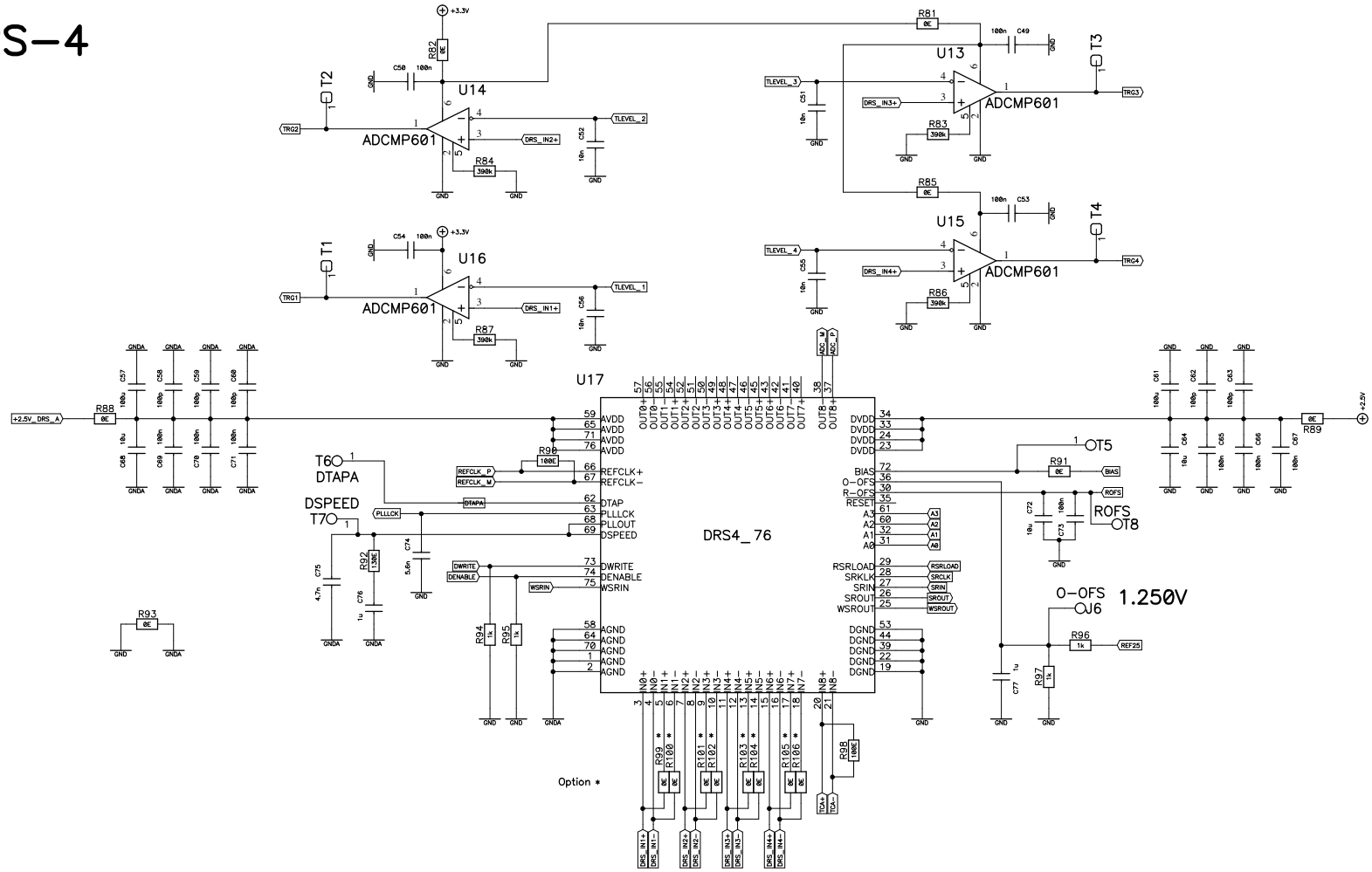
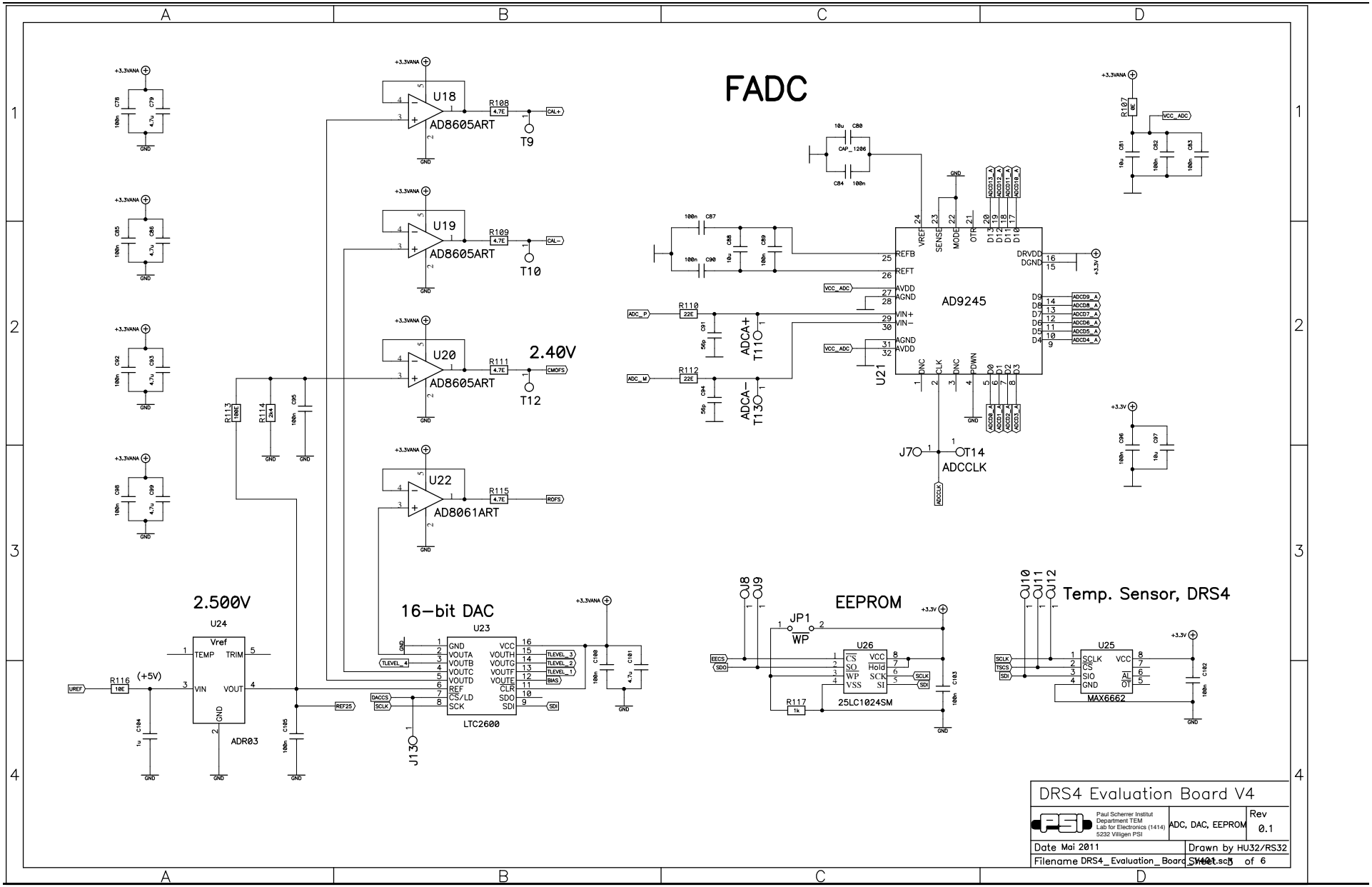
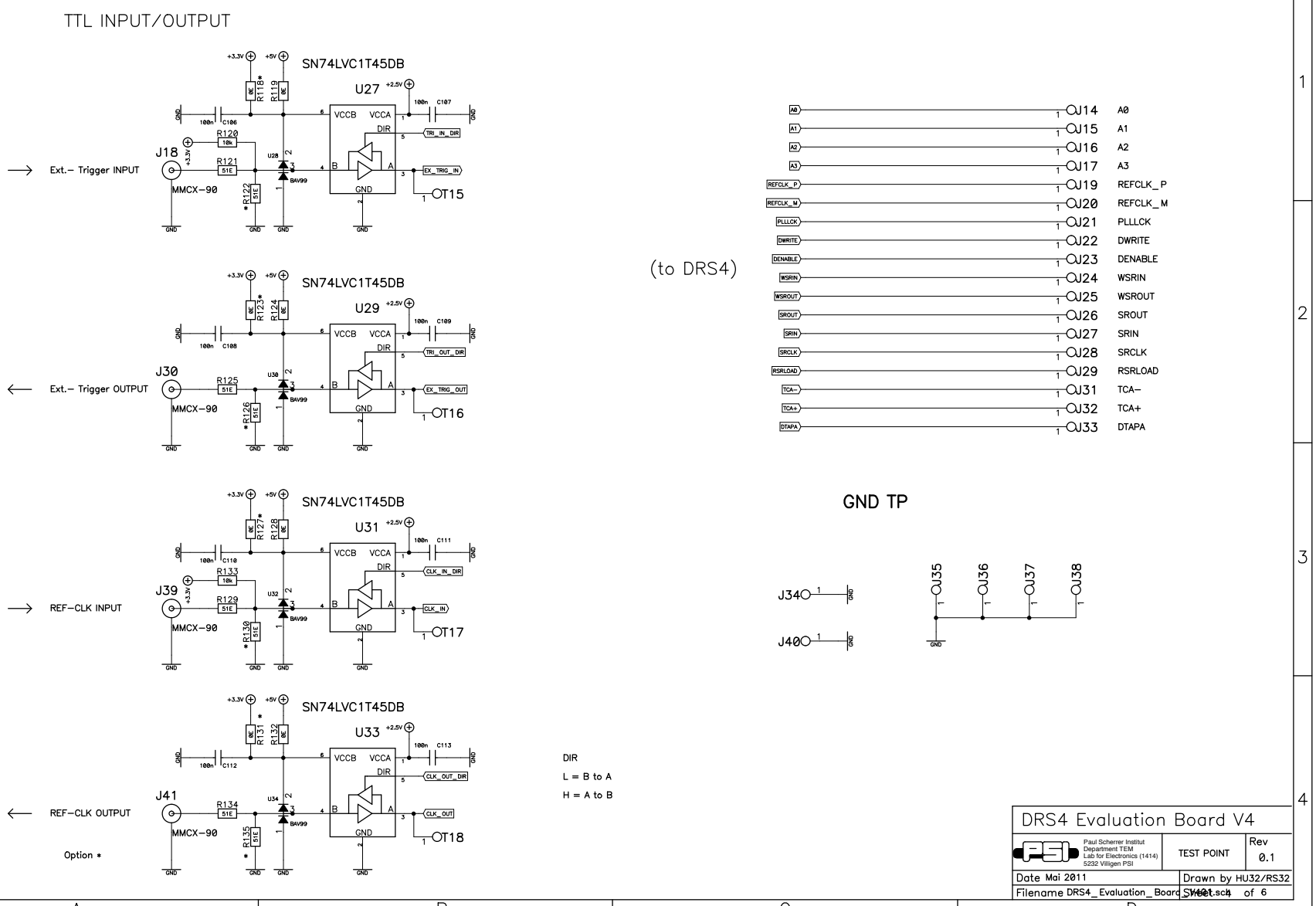
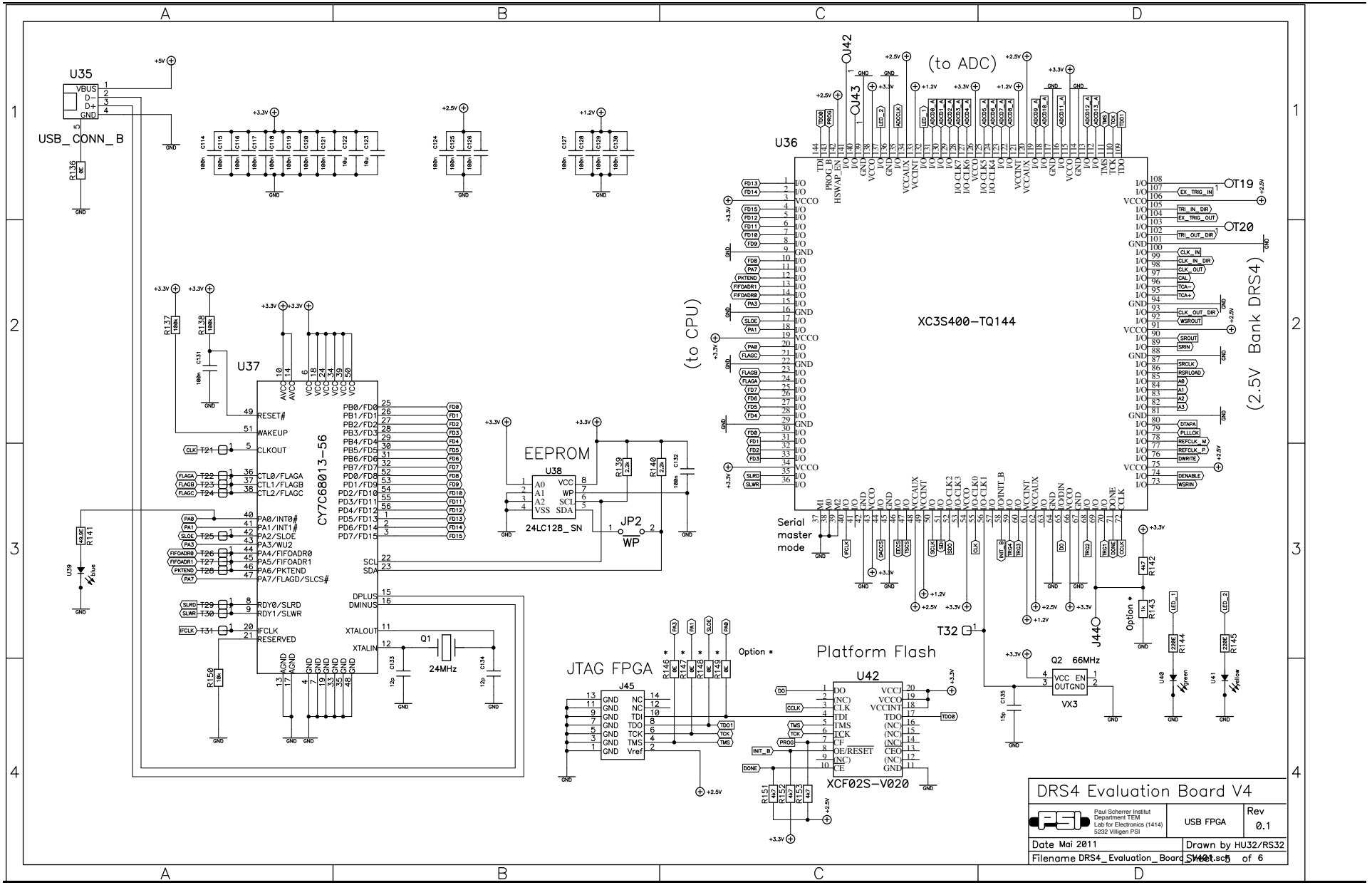
5. DRS4 Evaluation Board V4 Schematics

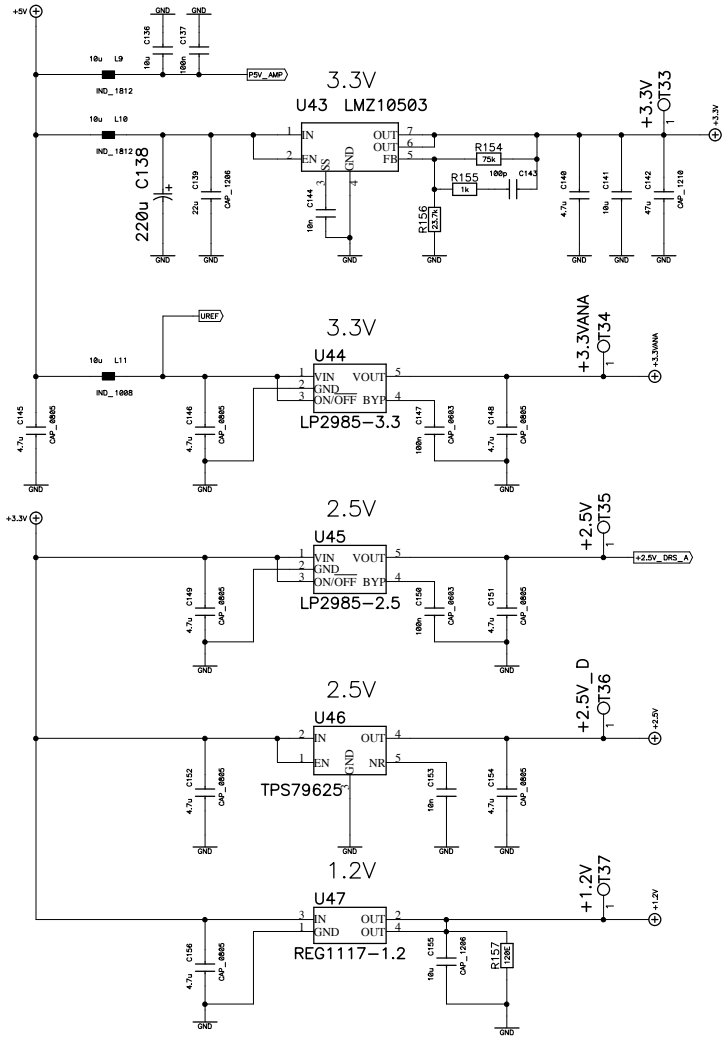



DRS–4
U13
U14
U15
U16
U17
ADCMP601
DRS4_76
T1
T2
T3
T4
T5
T6
T7
T8
DTAPA
DSPEED
ROFS
0–OFS
1.250V
Option *
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
DRS4
Rev
0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_SW01.sch
Sheet 2 of 6


FADC
U18
AD8605ART
U19
AD8605ART
U20
AD8605ART
2.40V
U22
AD8061ART
AD9245
U21
ADCA+
ADCA−
ADCCLK
2.500V
U24
ADR03
16−bit DAC
U23
LTC2600
EEPROM
JP1
WP
U26
25LC1024SM
Temp. Sensor, DRS4
U25
MAX6662
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
ADC, DAC, EEPROM
Rev
0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_SW401.sch
Sheet 5 of 6


TTL INPUT/OUTPUT
SN74LVC1T45DB
U27
J18
Ext.– Trigger INPUT
MMCX–90
R120
R121
R122
TRI_IN_DIR
EX_TRIG_IN
OT15
SN74LVC1T45DB
U29
J30
Ext.– Trigger OUTPUT
MMCX–90
R125
R126
TRI_OUT_DIR
EX_TRIG_OUT
OT16
SN74LVC1T45DB
U31
J39
REF–CLK INPUT
MMCX–90
R133
R129
R130
CLK_IN_DIR
CLK_IN
OT17
SN74LVC1T45DB
U33
J41
REF–CLK OUTPUT
MMCX–90
R134
R135
CLK_OUT_DIR
CLK_OUT
OT18
Option *
VCCB VCCA
DIR
GND
(to DRS4)
A0 J14 A0
A1 J15 A1
A2 J16 A2
A3 J17 A3
REFCLK_P J19 REFCLK_P
REFCLK_M J20 REFCLK_M
PLLLCK J21 PLLLCK
DWRITE J22 DWRITE
DENABLE J23 DENABLE
WSRIN J24 WSRIN
WSROUT J25 WSROUT
SROUT J26 SROUT
SRIN J27 SRIN
SRCLK J28 SRCLK
RSRLOAD J29 RSRLOAD
TCA– J31 TCA–
TCA+ J32 TCA+
DTAPA J33 DTAPA
GND TP
J34
J40
J35
J36
J37
J38
DIR
L = B to A
H = A to B
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
TEST POINT
Rev 0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_Sheet.sch
Sheet 4 of 6


U35
USB_CONN_B
U36
XC3S400-TQ144
(to ADC)
(to CPU)
(2.5V Bank DRS4)
U37
CY7C68013-56
EEPROM
U38
24LC128_SN
JP2
WP
Serial master mode
JTAG FPGA
J45
Platform Flash
U42
XCF02S-V020
Q1
24MHz
Q2 66MHz
VX3
Option *
T32
J44
DRS4 Evaluation Board V4
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
USB FPGA
Rev 0.1
Date Mai 2011
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_Sheet5.sch
Sheet 5 of 6



+3.3V CPU, FPGA, ADC (digital)

+3.3VANA ADC DAC

+2.5V AVDD DRS4 (analog)

+2.5V DVDD, DRS4, FPGA (digital)

+1.2V FPGA (INT)

FP1 FP_1MM

FP2 FP_1MM

HU32_11_2_2

DRS4 Evaluation Board V4		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	POWER	Rev 0.1
Date Mai 2011	Drawn by HU32/RS32	
Filename DRS4_Evaluation_Board_SW401.sch	Sheet 3 of 6	