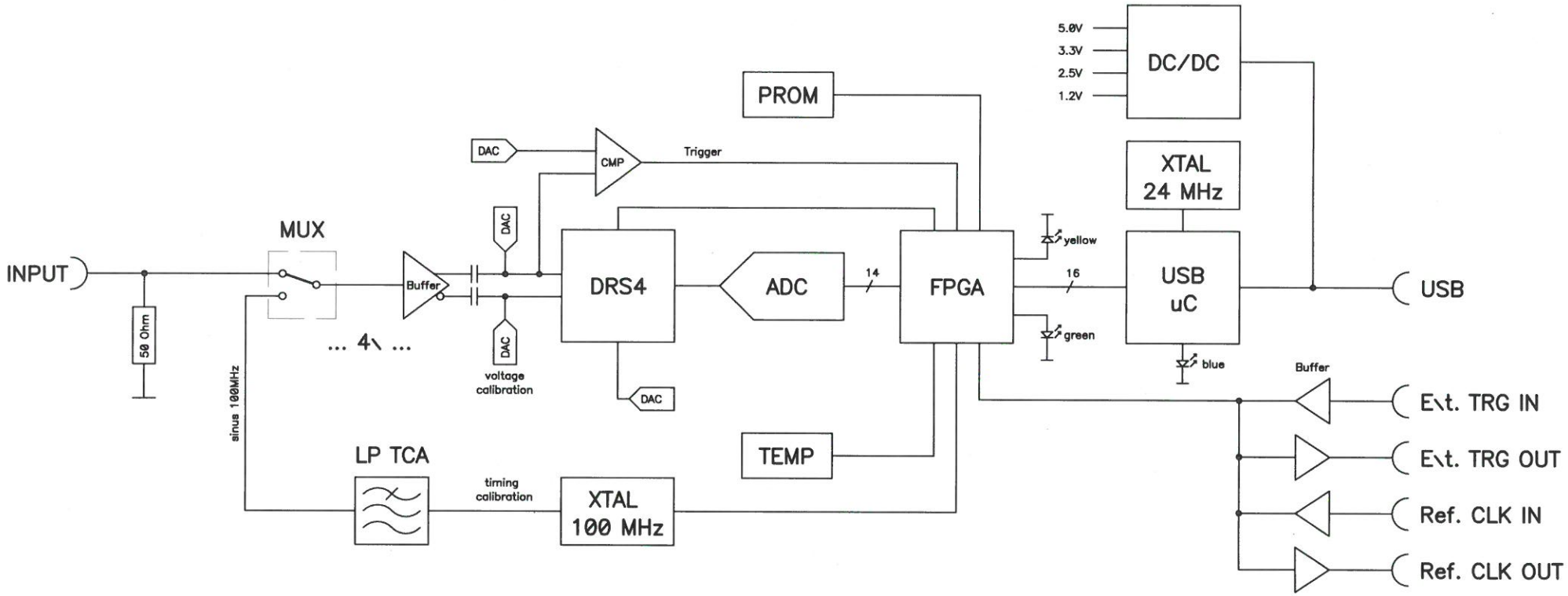
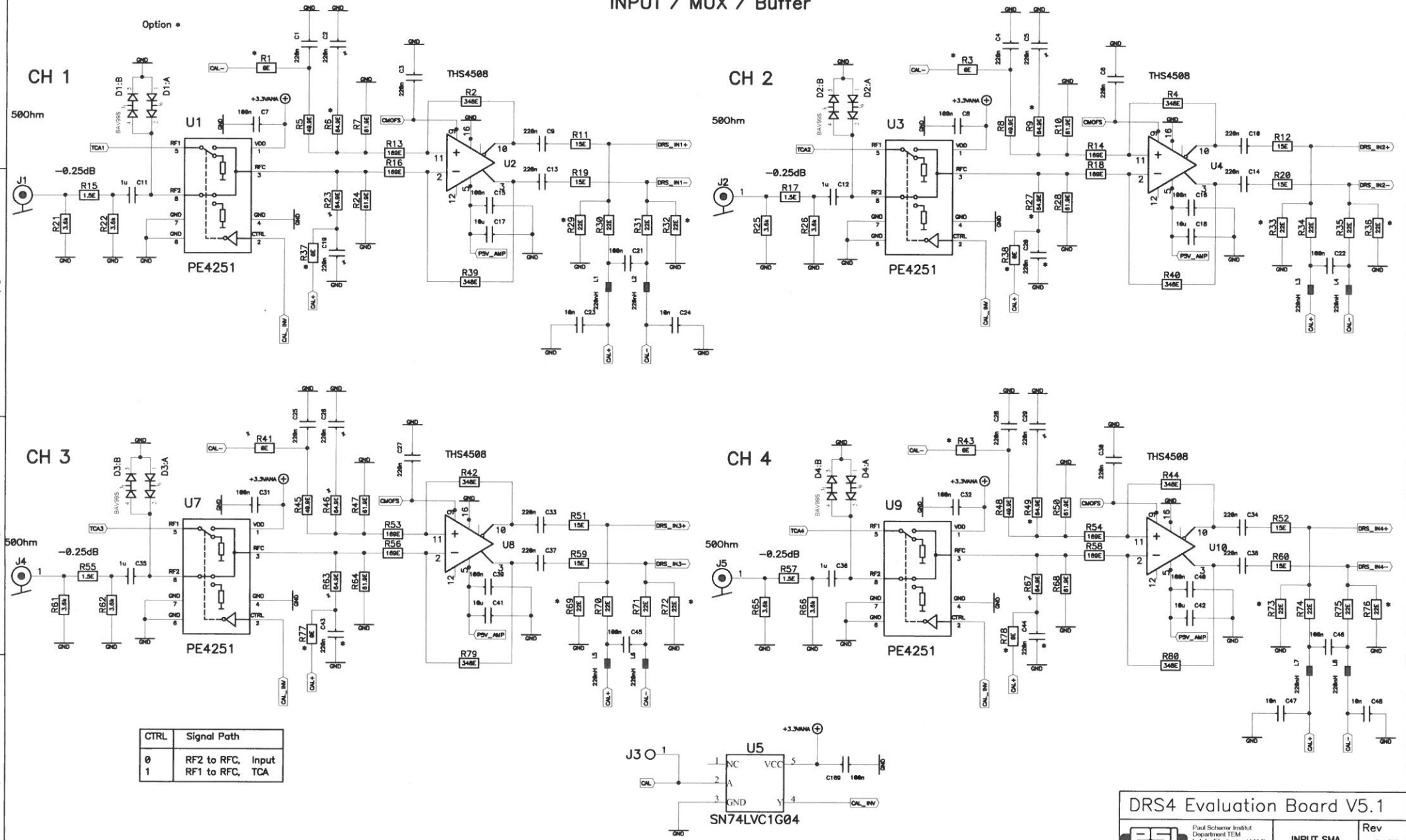
DRS4 Evaluation Board V5.1



DRS4 Evaluation Board V5.1

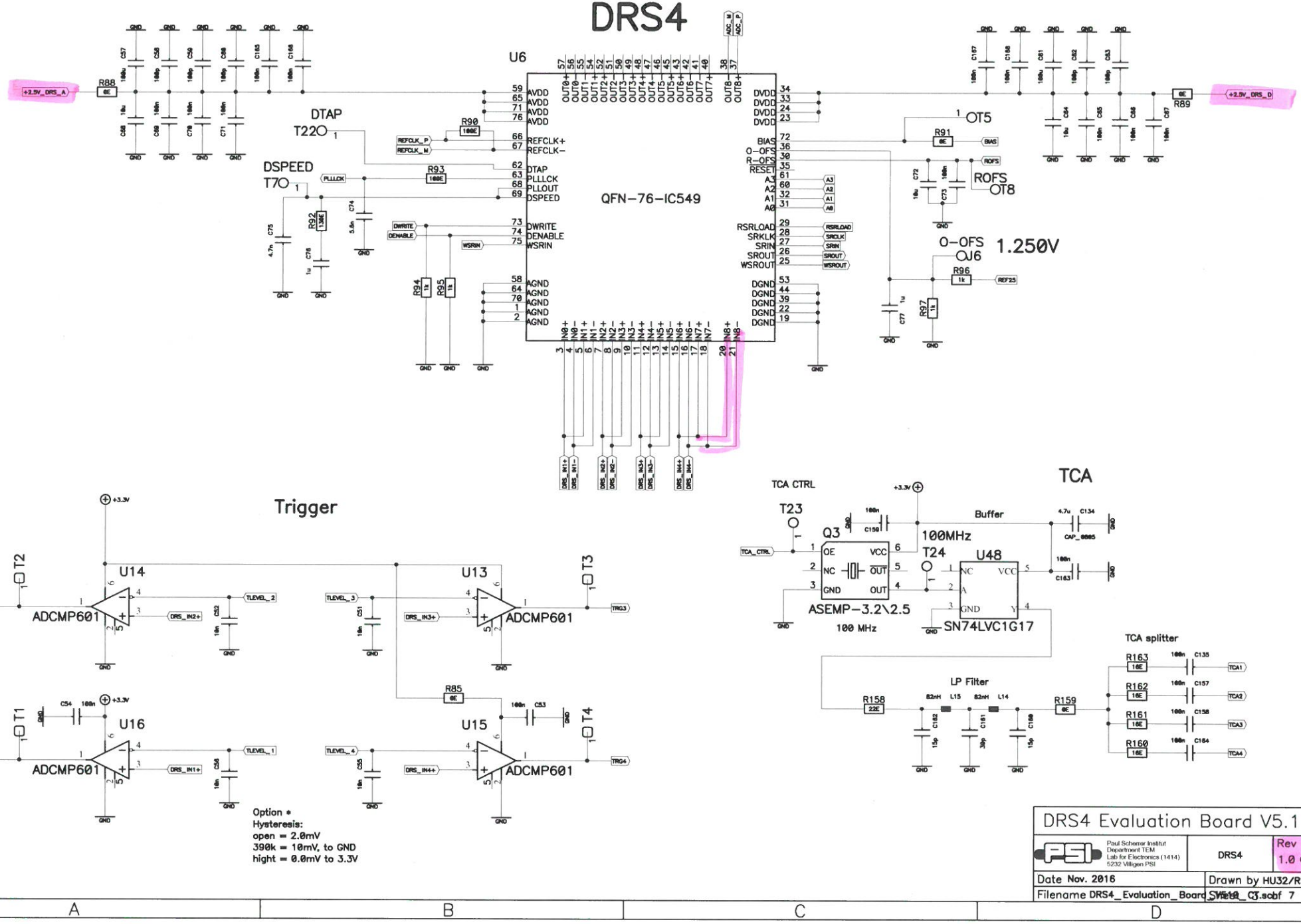
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	BLOCK DIAGRAM	Rev 1.0 CT
Date Nov. 2016		Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.1_CT.sch		Sheet 7

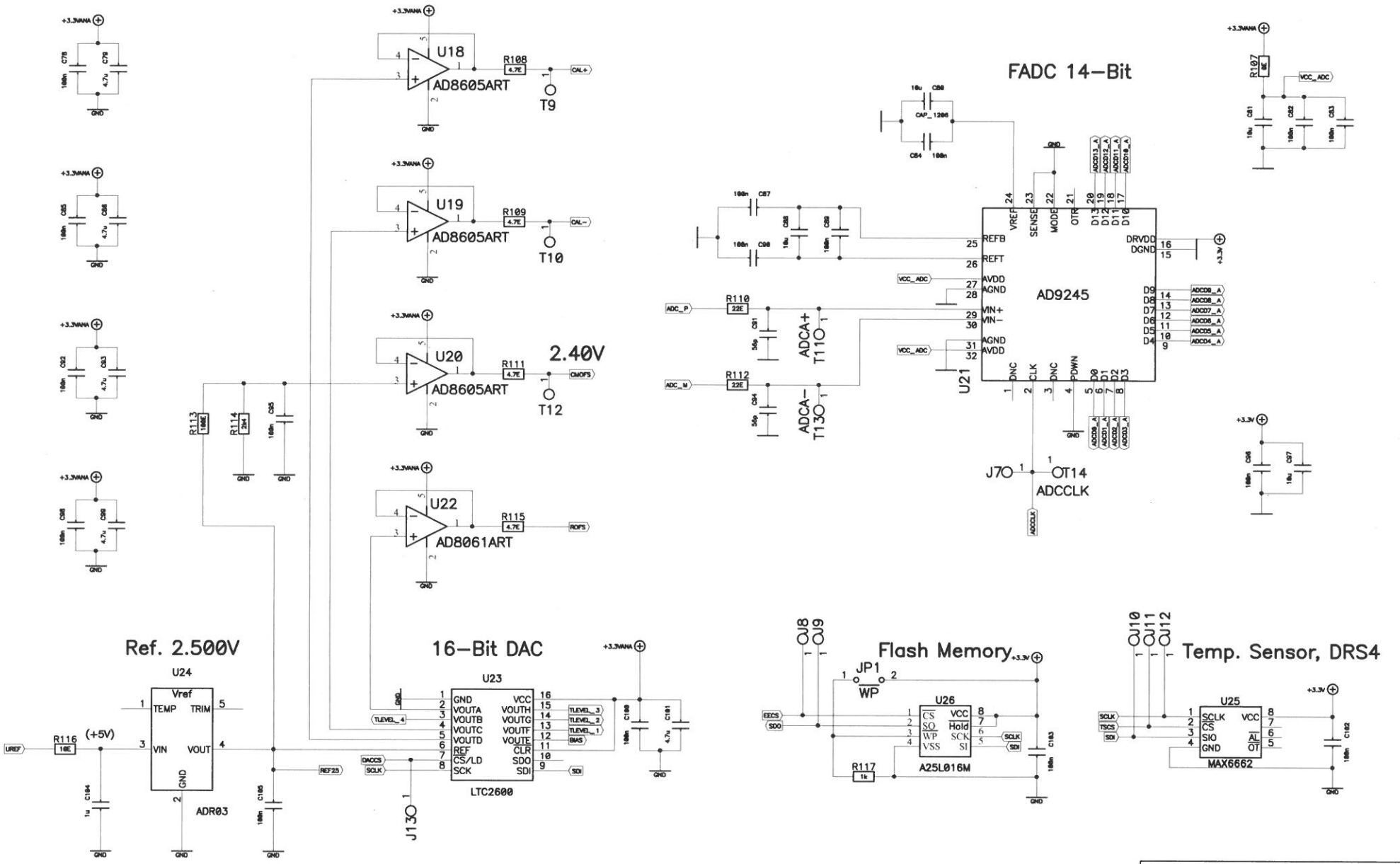
INPUT / MUX / Buffer



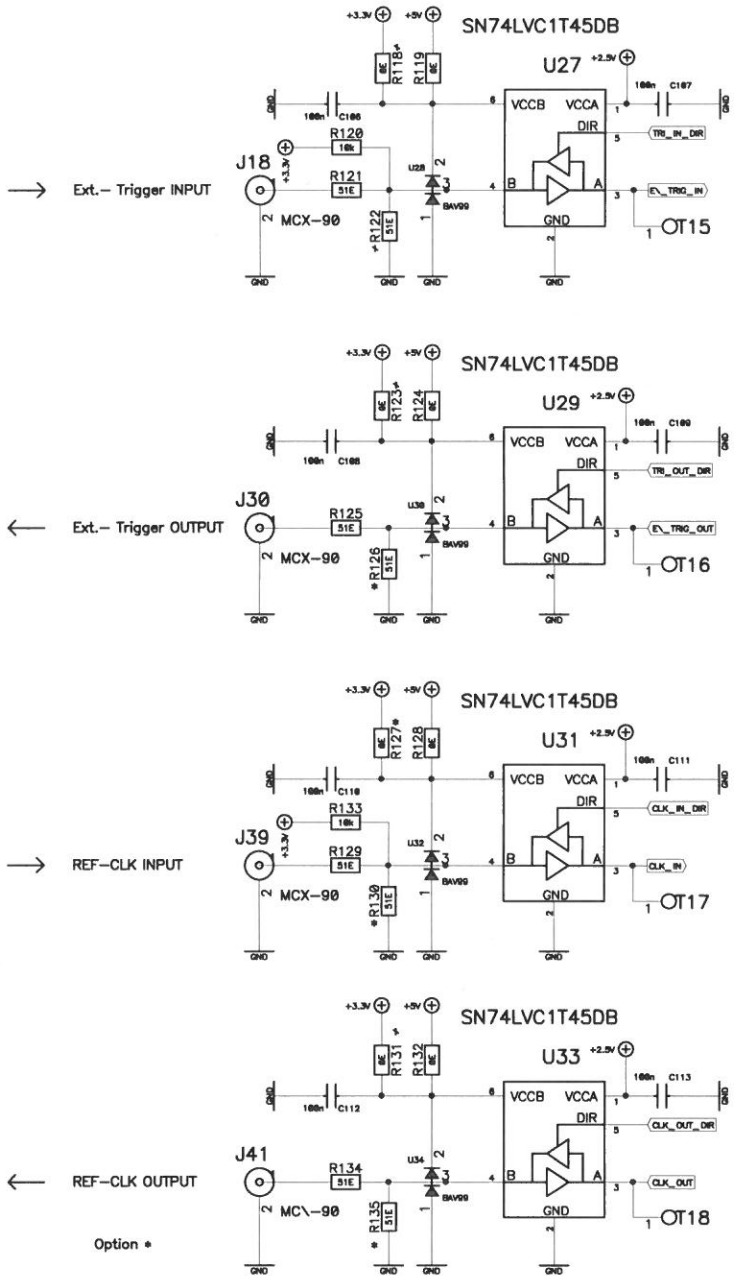
CTRL	Signal Path
0	RF2 to RFC, Input
1	RF1 to RFC, TCA

DRS4 Evaluation Board V5.1		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	INPUT SMA	Rev 1.0 CT
Date Nov. 2016		Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.0_CT.sch		Sheet 7


DRS4
U6
QFN-76-IC549
DTAP
T22
DSPEED
T7
OT5
ROFS
OT8
O-OFS
OJ6
1.250V
Trigger
U14
U13
U16
U15
ADCMP601
TCA
TCA CTRL
T23
Q3
ASEMP-3.2\2.5
100 MHz
100MHz
Buffer
T24
U48
SN74LVC1G17
TCA splitter
LP Filter
Option *
Hysteresis:
open = 2.0mV
390k = 10mV, to GND
hight = 0.0mV to 3.3V
DRS4 Evaluation Board V5.1
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
DRS4
Rev
1.0 CT
Date Nov. 2016
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.1_C3.sch

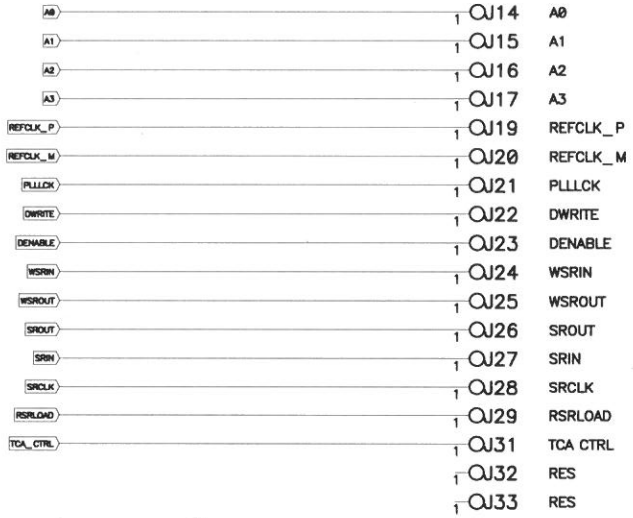

FADC 14-Bit
AD9245
U21
U18
U19
U20
U22
AD8605ART
AD8605ART
AD8605ART
AD8061ART
R108
R109
R111
R115
CAL+
CAL-
CMOFS
ROFS
T9
T10
T12
2.40V
R110
R112
ADC_P
ADC_M
ADCA+
ADCA-
T11
T13
J7
OT14
ADCCLK
R107
VCC_ADC
Ref. 2.500V
U24
ADR03
R116
(+5V)
VREF
REF25
16-Bit DAC
U23
LTC2600
DACCS
SCLK
J13
Flash Memory
JP1
WP
U26
A25L016M
R117
EECS
SDO
SDI
Temp. Sensor, DRS4
U25
MAX6662
SCLK
TSCS
SDI
DRS4 Evaluation Board V5.1
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
ADC, DAC, EEPROM
Rev
1.0 CT
Date Nov. 2016
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.1.0_CT.sch
Sheet 7

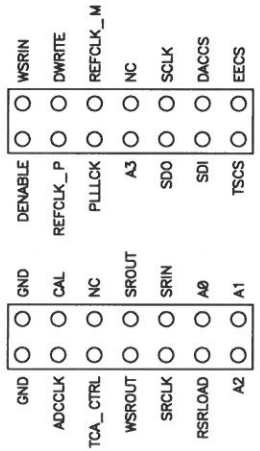
TTL INPUT/OUTPUT



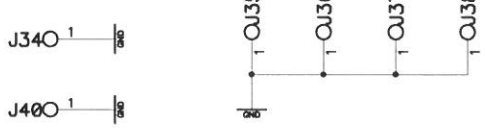
DIR
L = B to A
H = A to B

(to DRS4)

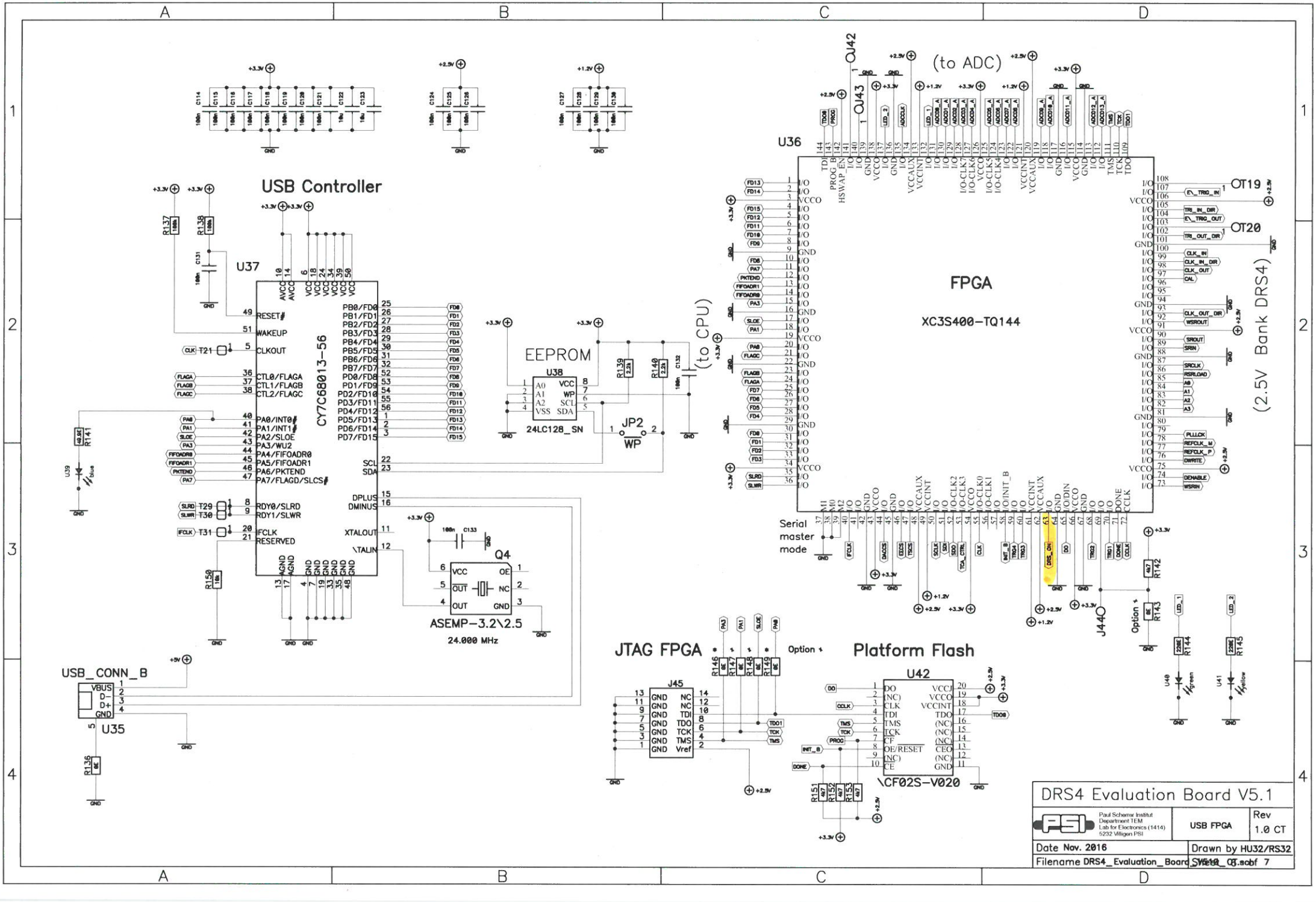


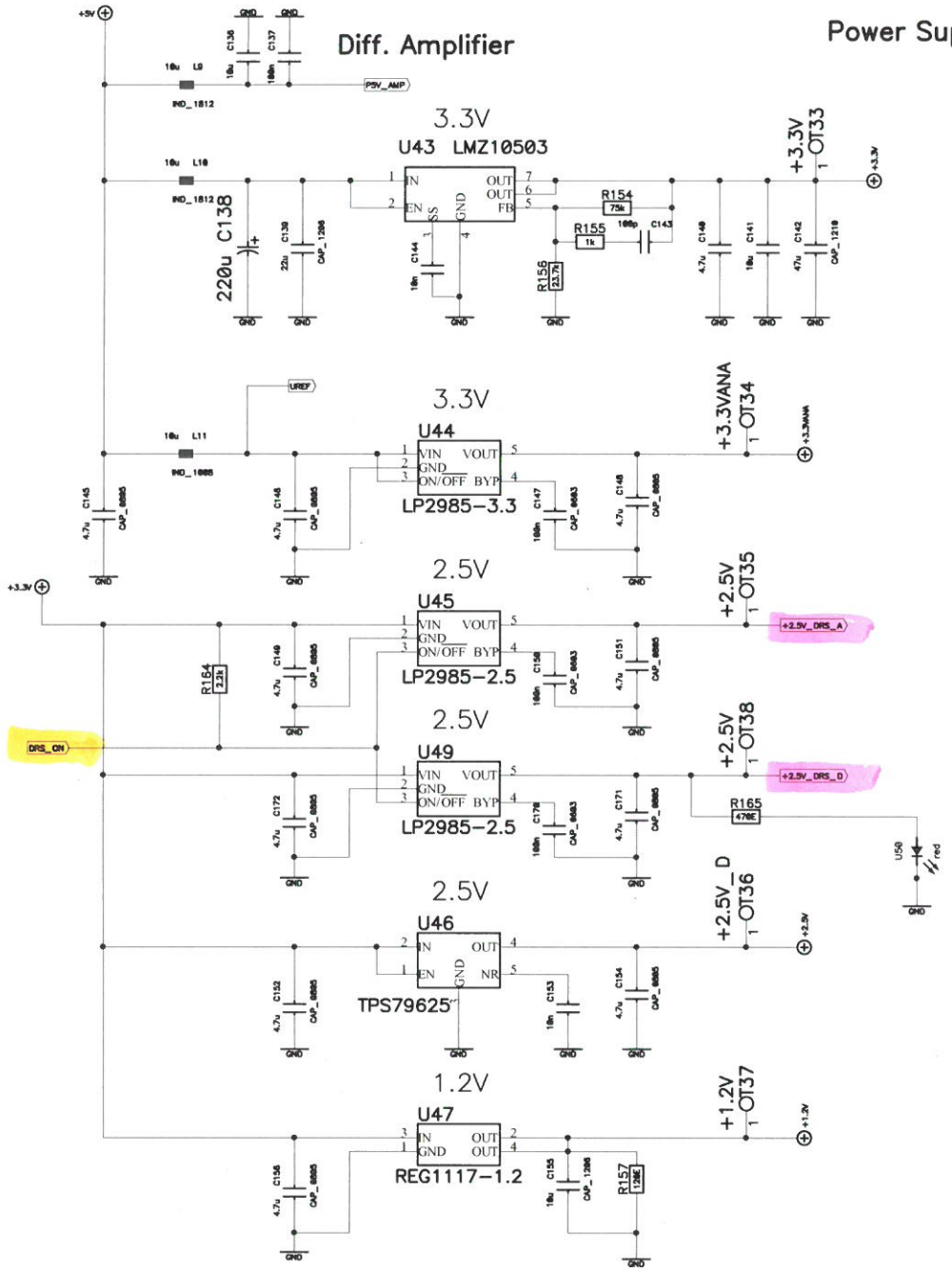


GND TP



DRS4 Evaluation Board V5.1		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	IN OUT TEST POINT	Rev 1.0 CT
Date Nov. 2016	Drawn by HU32/RS32	
Filename DRS4_Evaluation_Board_V5.1_CT.sch	Sheet 7	


USB Controller
U37
CY7C68013-56
EEPROM
U38
24LC128_SN
JP2
WP
(to CPU)
(to ADC)
U36
FPGA
XC3S400-TQ144
(2.5V Bank DRS4)
Serial master mode
OT19
OT20
Q4
ASEMP-3.2\2.5
24.000 MHz
USB_CONN_B
U35
JTAG FPGA
J45
Platform Flash
U42
\CF02S-V020
J44
Option *
DRS Evaluation Board V5.1
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
USB FPGA
Rev 1.0 CT
Date Nov. 2016
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.1_USB_FPGA.schdoc
Sheet 7 of 7


Diff. Amplifier
Power Supplies
3.3V
U43 LMZ10503
+3.3V
OT33
220u C138
R154
75k
R155
1k
R156
23.7k
3.3V
U44
LP2985-3.3
+3.3VANA
OT34
2.5V
U45
LP2985-2.5
+2.5V
OT35
+2.5V_DRS_A
R164
2.2k
DRS_ON
2.5V
U49
LP2985-2.5
+2.5V
OT38
+2.5V_DRS_D
R165
470E
U50
red
2.5V
U46
TPS79625
+2.5V_D
OT36
1.2V
U47
REG1117-1.2
+1.2V
OT37
+3.3V CPU, FPGA, TCA, PROM, ADC (digital)
+3.3VANA ADC DAC OPAMP
+2.5V AVDD DRS4 (analog)
+2.5V DVDD DRS4 (digital)
DRS ON !
+2.5V DVDD, FPGA (digital)
+1.2V FPGA (INT)
FP1
FP_1MM
FP2
FP_1MM
HU32_16_2_3
DRS4 Evaluation Board V5.1
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
POWER
Rev
1.0 CT
Date Nov. 2016
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.1_CT.sch
Sheet 7