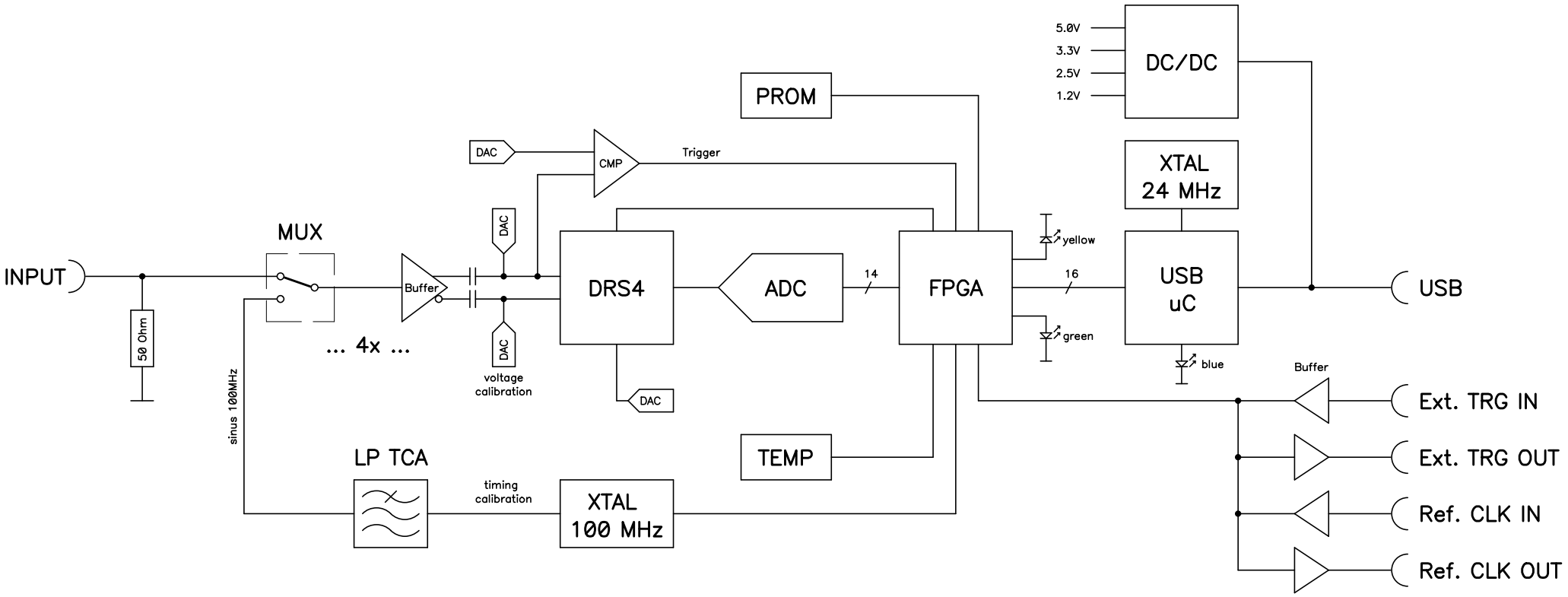
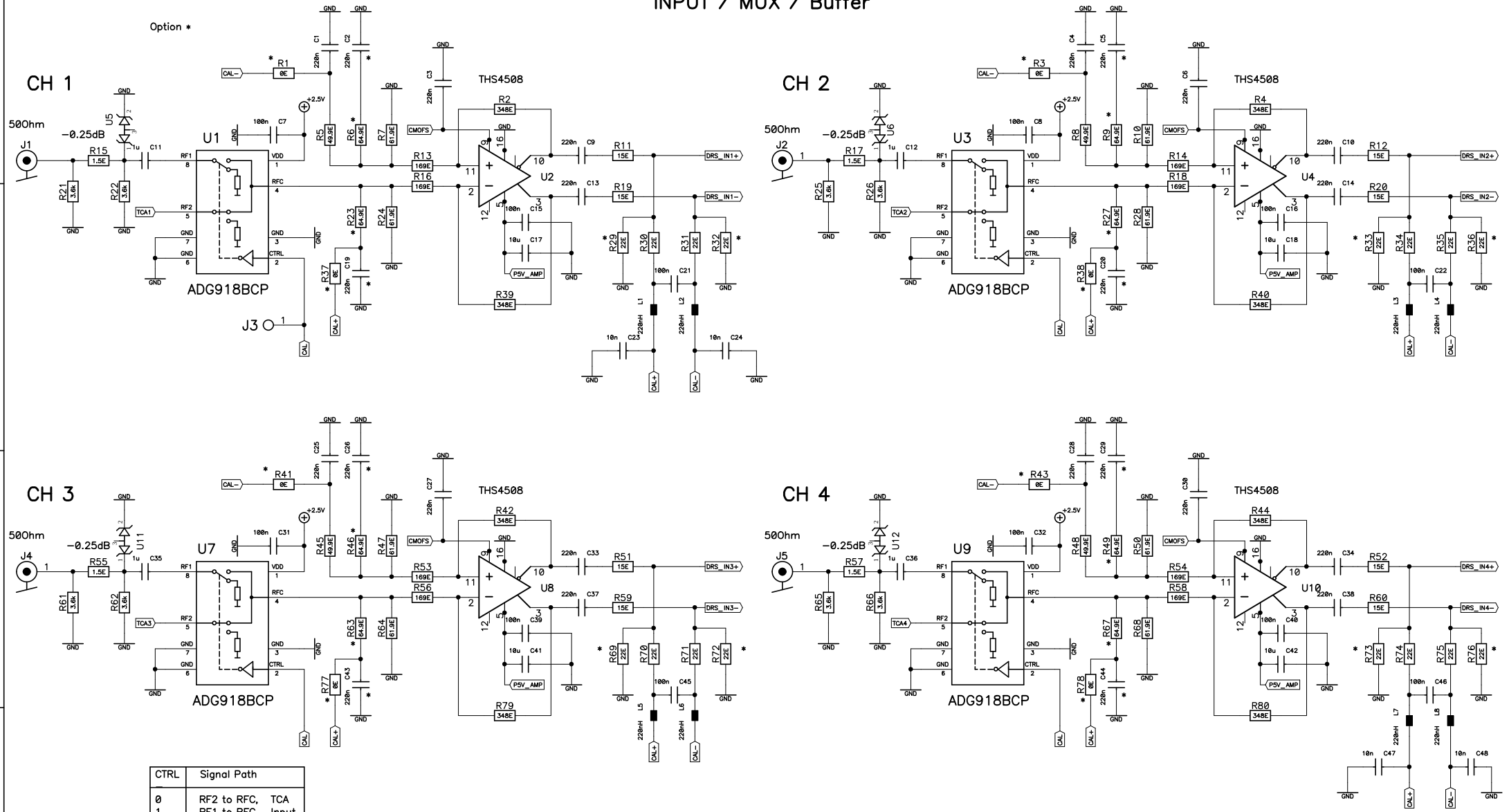
DRS4 Evaluation Board V5



DRS4 Evaluation Board V5		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	BLOCK DIAGRAM	Rev 0.4
Date Nov. 2013		Drawn by HU32/RS32
Filename DRS4_ Evaluation_ Board_V5.sch		Sheet 1 of 7

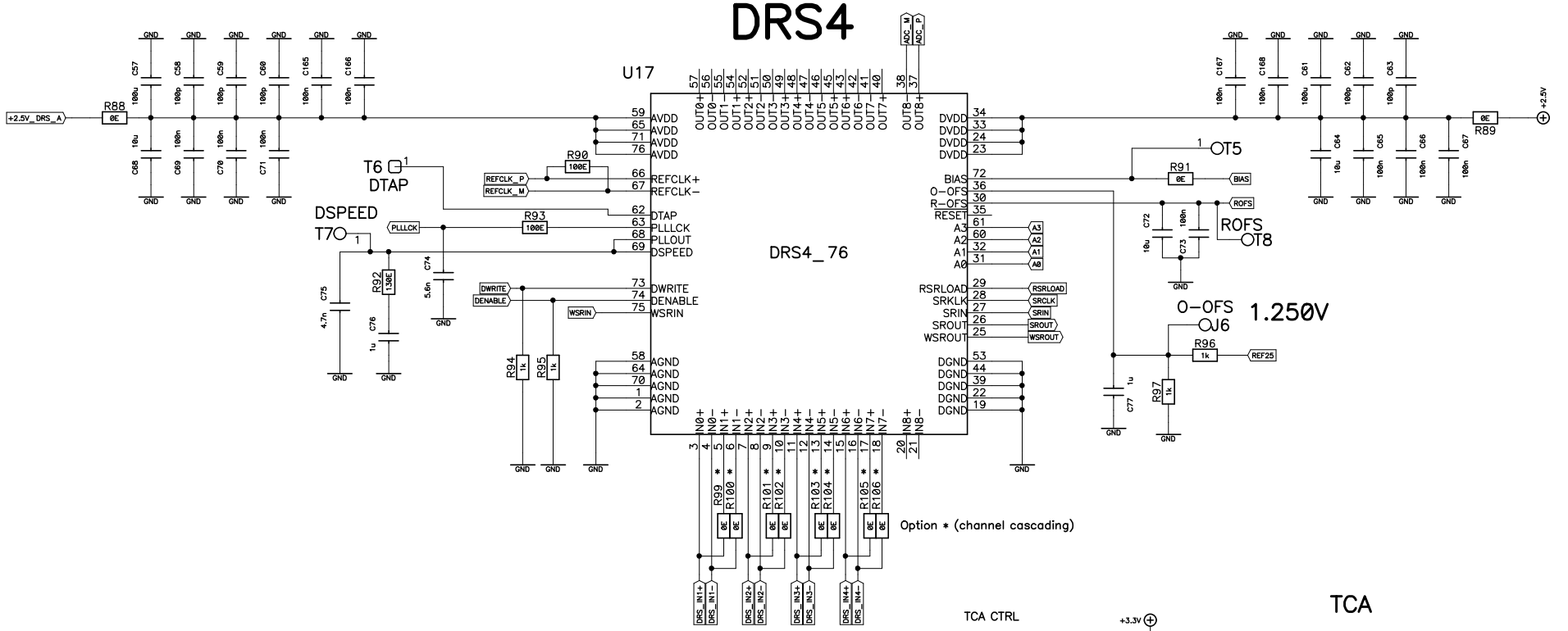
INPUT / MUX / Buffer



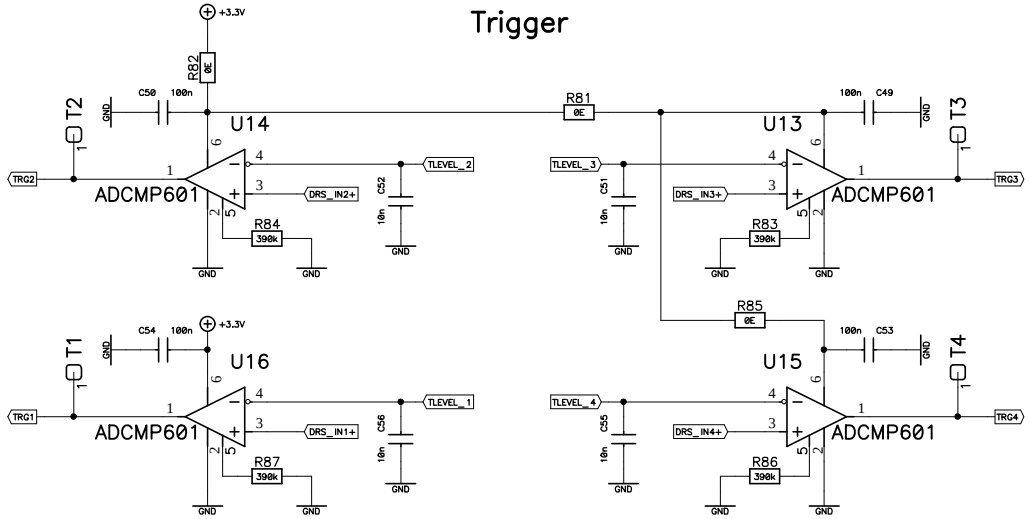
CTRL	Signal Path
0	RF2 to RFC, TCA
1	RF1 to RFC, Input

DRS4 Evaluation Board V5		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	INPUT SMA	Rev 0.4
Date Nov. 2013		Drawn by HU32/RS32
Filename DRS4_ Evaluation_ Board_V5_1.sch		Sheet 2 of 7

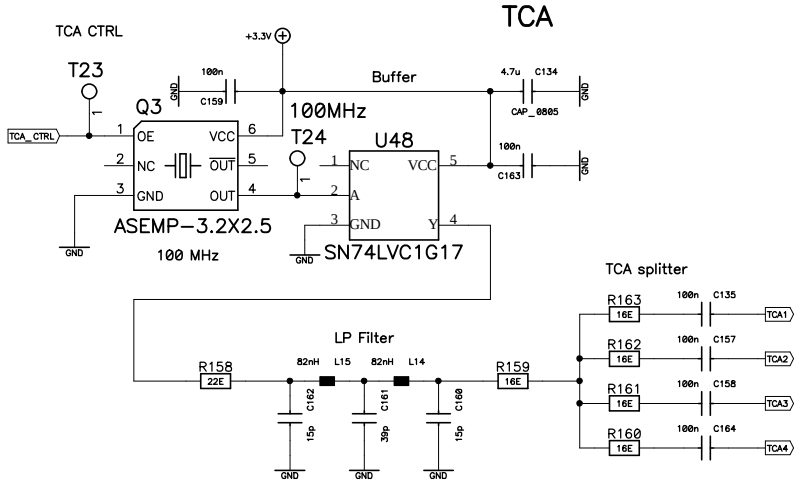
DRS4



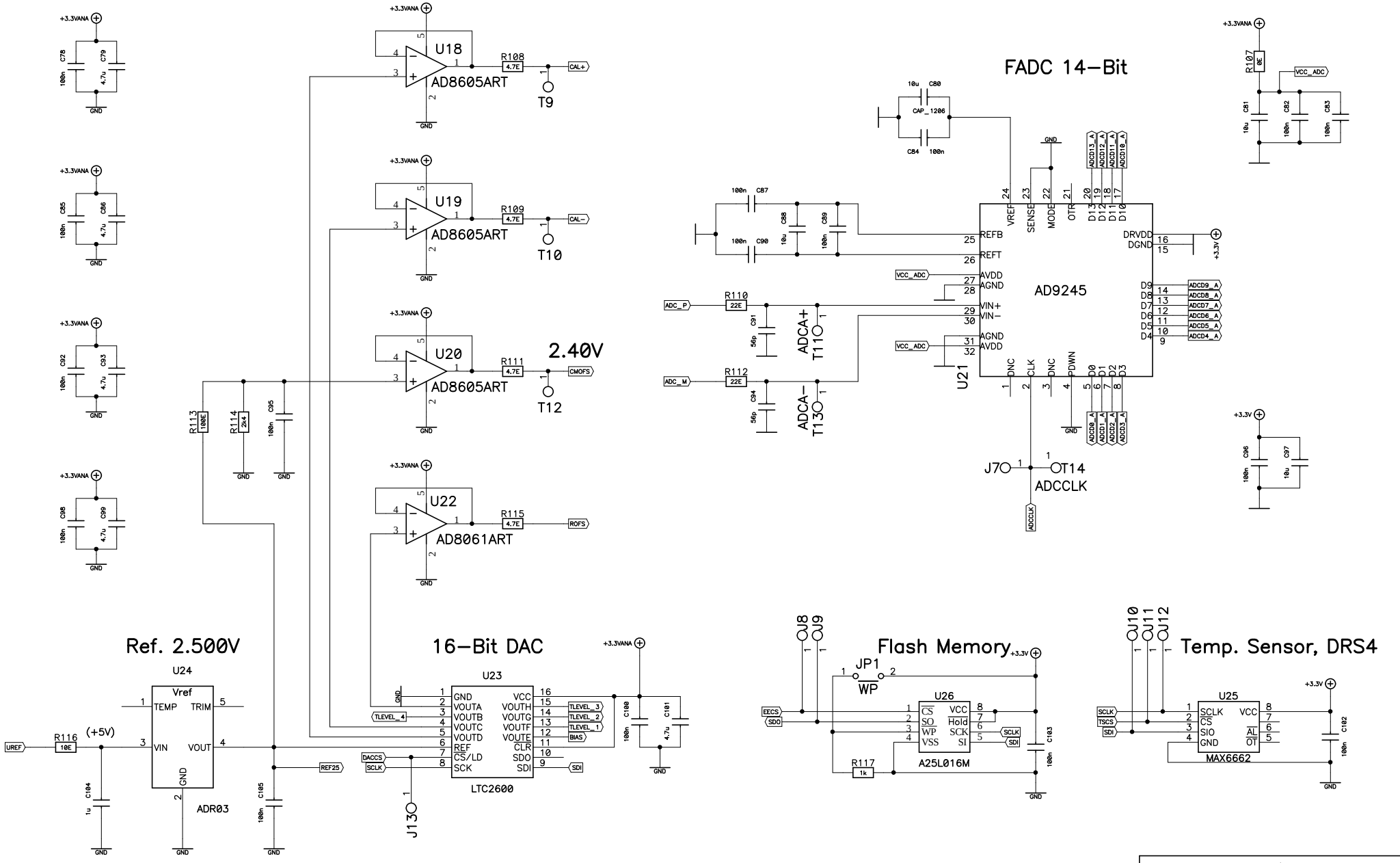
Trigger



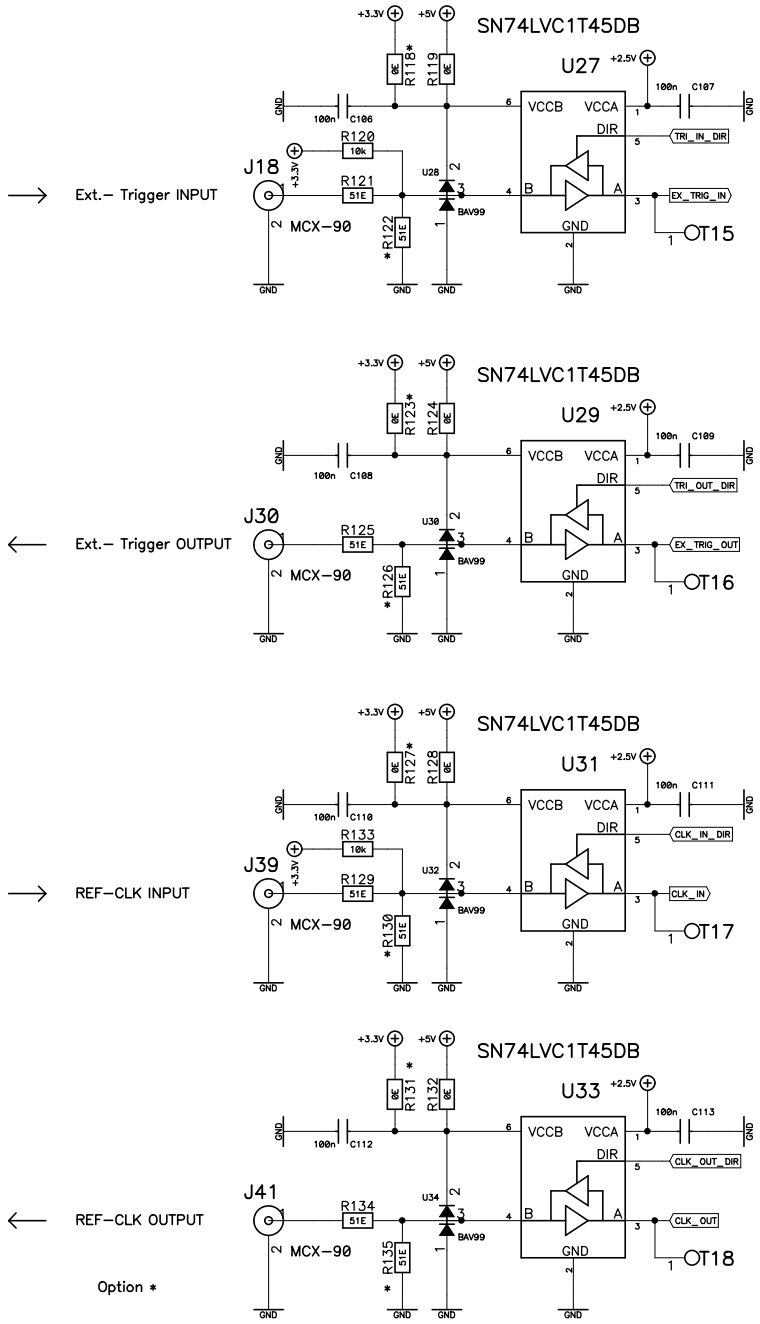
TCA



DRS4 Evaluation Board V5		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	DRS4	Rev 0.4
Date Nov. 2013		Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5.sch		Sheet 5 of 7


FADC 14-Bit
AD9245
U21
U18
U19
U20
U22
AD8605ART
AD8605ART
AD8605ART
AD8061ART
2.40V
T9
T10
T12
CAL+
CAL-
CMOFS
ROFS
ADCA+
ADCA-
T11
T13
J7
T14
ADCCLK
Ref. 2.500V
U24
ADR03
(+5V)
REF25
16-Bit DAC
U23
LTC2600
J13
Flash Memory
U26
A25L016M
JP1
WP
J8
J9
Temp. Sensor, DRS4
U25
MAX6662
J10
J11
J12
DRS4 Evaluation Board V5
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
ADC, DAC, EEPROM
Rev
0.4
Date Nov. 2013
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5_4.sch
Sheet 4 of 7

TTL INPUT/OUTPUT

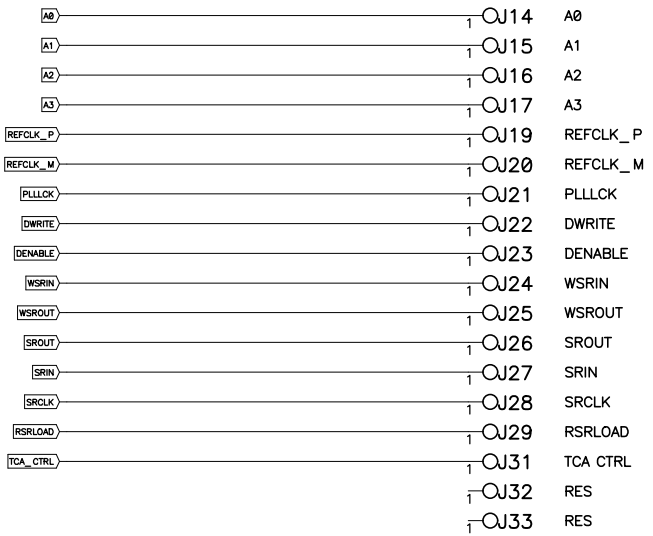


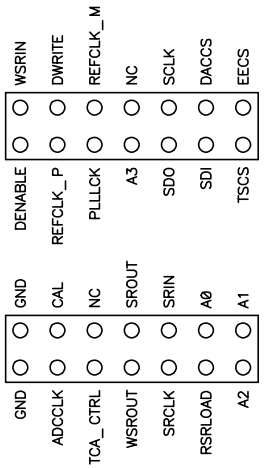
DIR

L = B to A

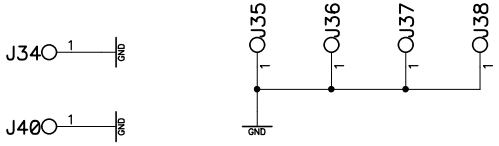
H = A to B

(to DRS4)

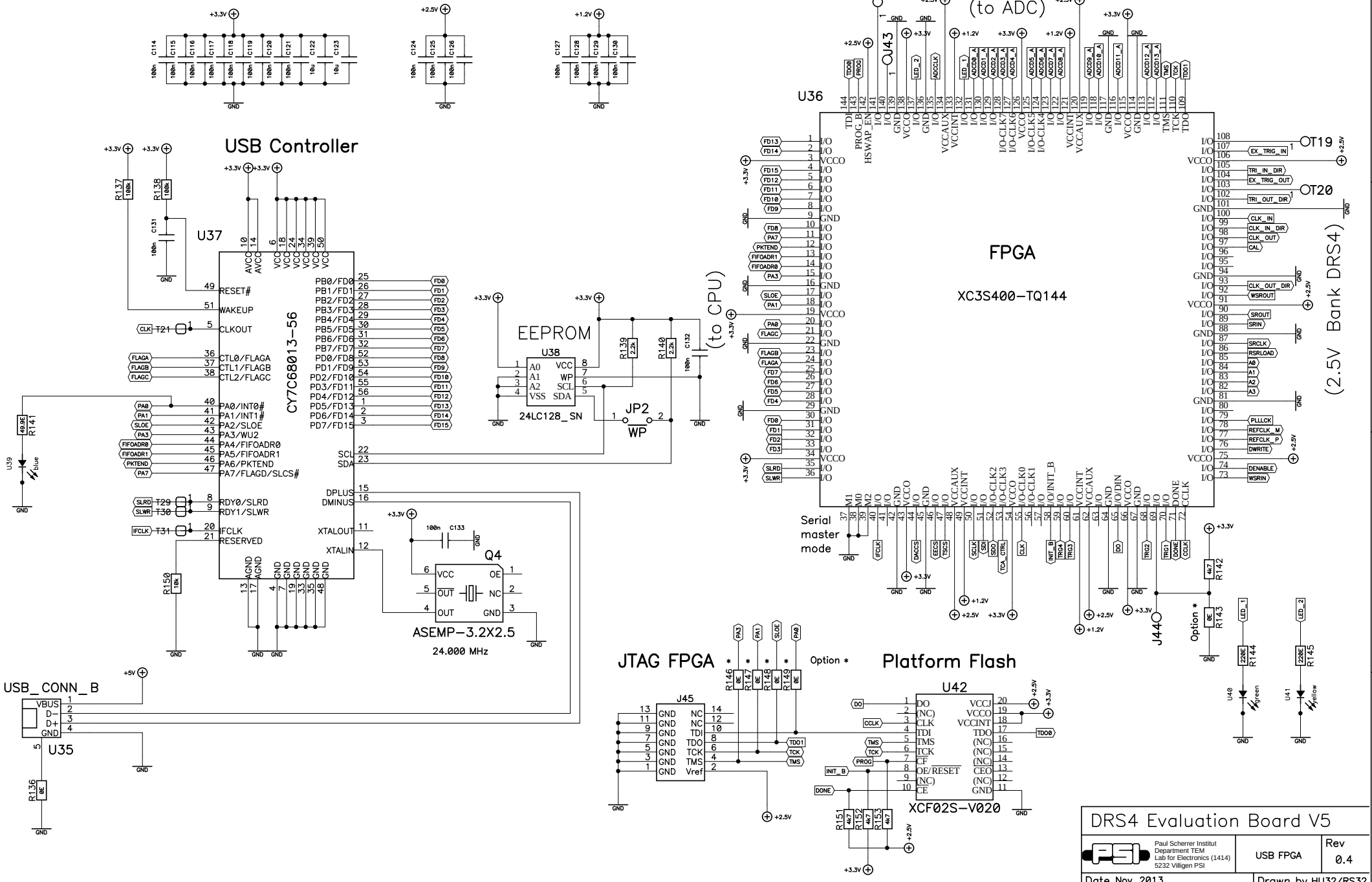


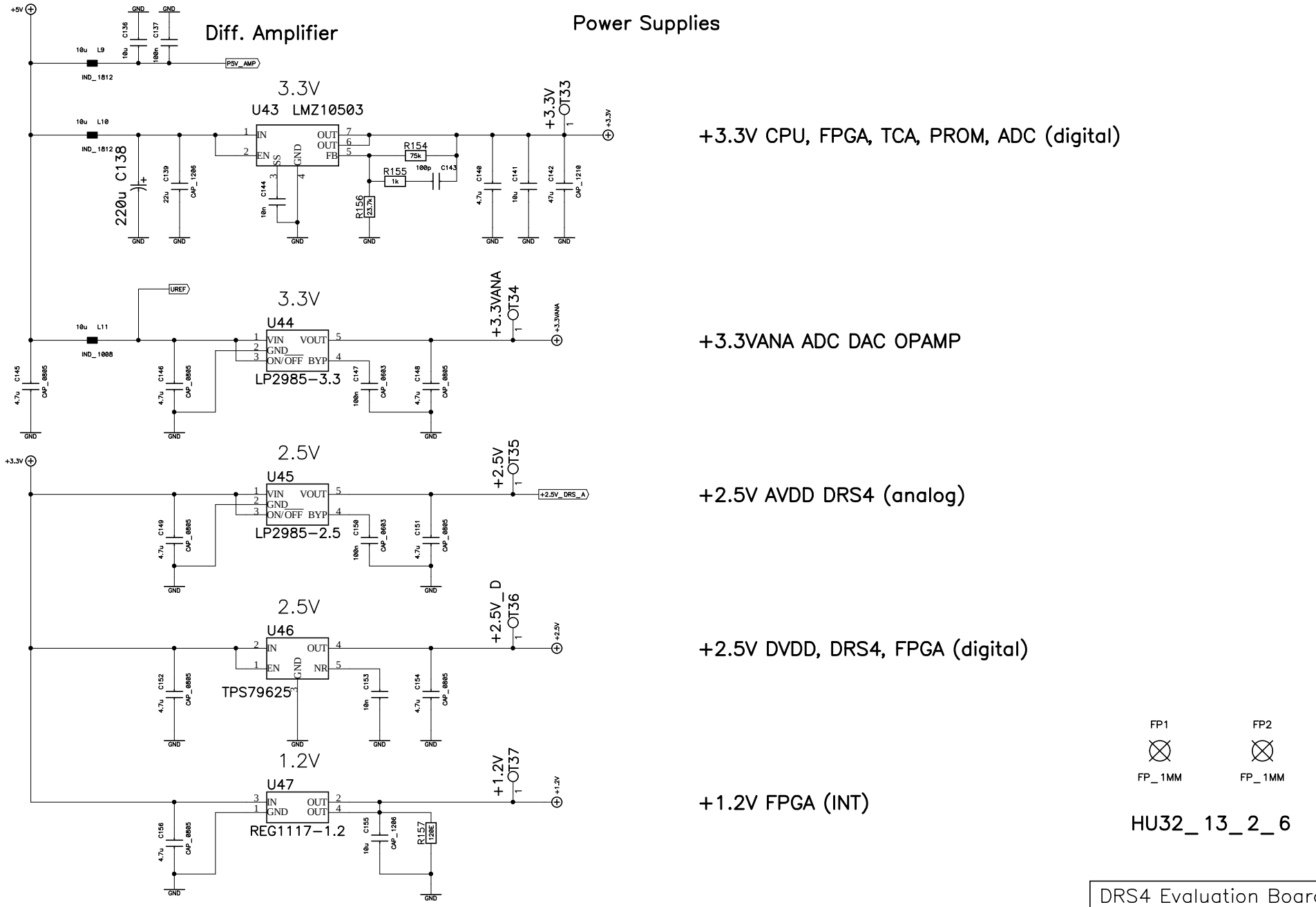


GND TP



DRS4 Evaluation Board V5		
Paul Scherrer Institut Department TEM Lab for Electronics (1414) 5232 Villigen PSI	IN OUT TEST POINT	Rev 0.4
Date Nov. 2013	Drawn by HU32/RS32	
Filename DRS4_ Evaluation_ Board_V5_4.sch	Sheet 5 of 7	


USB Controller
U37
CY7C68013-56
RESET#
WAKEUP
CLKOUT
CTL0/FLAGA
CTL1/FLAGB
CTL2/FLAGC
PA0/INT0#
PA1/INT1#
PA2/SLOE
PA3/WU2
PA4/FIFOADR0
PA5/FIFOADR1
PA6/PKTEND
PA7/FLAGD/SLCS#
RDY0/SLRD
RDY1/SLWR
IFCLK
RESERVED
XTALOUT
XTALIN
DPLUS
DMINUS
SCL
SDA
EEPROM
U38
24LC128_SN
WP
JP2
(to CPU)
FPGA
XC3S400-TQ144
U36
(to ADC)
(2.5V Bank DRS4)
Serial master mode
JTAG FPGA
J45
Platform Flash
U42
XCF02S-V020
Option *
USB_CONN_B
U35
ASEMP-3.2X2.5
24.000 MHz
Q4
J44
U39
blue
U40
green
U41
yellow
DRS4 Evaluation Board V5
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
USB FPGA
Rev 0.4
Date Nov. 2013
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V504.sch
Sheet 3 of 7


Diff. Amplifier
Power Supplies
3.3V
U43 LMZ10503
+3.3V CPU, FPGA, TCA, PROM, ADC (digital)
3.3V
U44
LP2985-3.3
+3.3VANA ADC DAC OPAMP
2.5V
U45
LP2985-2.5
+2.5V AVDD DRS4 (analog)
2.5V
U46
TPS79625
+2.5V DVDD, DRS4, FPGA (digital)
1.2V
U47
REG1117-1.2
+1.2V FPGA (INT)
FP1
FP2
FP_1MM
FP_1MM
HU32_13_2_6
DRS4 Evaluation Board V5
Paul Scherrer Institut
Department TEM
Lab for Electronics (1414)
5232 Villigen PSI
POWER
Rev 0.4
Date Nov. 2013
Drawn by HU32/RS32
Filename DRS4_Evaluation_Board_V5_1.sch
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